



ENHANCED PLC TRANSCEIVER DESIGN WITH LOW POWER AND DENSITY

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ABSTRACT:

Today's VLSI technology is advancing in such a way that the designers can incorporate a large number of functions inside a chip. As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited number of available I/O pins. The PLC is one in which the power pins and the power distribution networks of ICs are used for data communication as well as power delivery. PLC is used in order to reduce the number of input pins that an IC needs to couple the test data signals to each and every node. Hence to extract the test data signals from this power lines, so many receivers are in need at each and every nodes of the ICs or at places where we have to apply the test. A PLC receiver presented in this paper intends to demonstrate the proof of concept, specifically the transmission of data through power lines. The main design objective of the proposed PLC receiver is the robust operation under variations and droops of the supply voltage rather than high data speed., Further, this concept is enhanced by using modified Schmitt trigger.

INTRODUCTION: Today's VLSI technology is advancing in such a way that the designers can incorporate a large number of functions inside a chip. Microprocessors are one of the best examples for this. Day by day the size of ICs reduces and the operations it can perform are increasing. So many challenges still exist such as, the need of proper provision for the thermally generated heat removal, the number of the input output pins that an IC needs, proper power supply injection etc., due to which there exists limits on incorporating functions inside ICs. Also routing inside the IC too has a major role in it. There should also be the provisions in ICs like sensors to detect what is happening inside each and every point and if anything happens wrongly, the normal state have to be recovered. Even though the increase in system complexity is an advantage in the sense that the size of ICs can be reduced, with that there should be new inventions for proper data passage inside the same. The power line communication aspect presented in this paper is one of such methods. In power line communication, it efficiently uses the power distribution networks inside ICs since they are the only components that reach each and every node. So if there have a provision to pass the test data, which are used for fault diagnosis, scan design etc. to whichever areas we need to apply the test that will be

an attractive way of communication in ICs, So that the routing overhead inside the ICs to pass these testing data can be intelligently avoided. So in PLC, the power distribution networks are used for power delivery and also data communication. The test data are superimposed on the power signal and are transmitted through the power distribution networks of ICs rather than the separately allotted routing paths. Also the number of power pins can be reduced since there is no need to carry the test data through the input pins. Of course, adopting such a power line communication always has to overcome the extreme noise level at the power lines. So there should be effective methods to overcome the same. Essentially there is the need of receivers at each and every node to extract these data signals efficiently from the power lines.

POWER LINE COMMUNICATION SYSTEMS IN VLSI CIRCUITS:

Power line communication (PLC) in VLSI circuits was proposed by Dr. Dong Ha's group to control internal nodes of an IC [2]-[6]. A PLC system achieves communications between an external control module and one or multiple internal nodes of an IC through the power distribution network. The goal of the proposed research is to reduce the cost of complex

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ICs through reduction of the number of pins required to control internal nodes. The external transmitter of our PLC system superimposes the data on the power supply and sends the data through a power pin(s) and the power distribution network of the IC to an internal node(s) without affecting the performance of the chip. The PLC receiver at an intended node extracts the data from the power distribution network. Each receiving node has a pre-assigned unique identification code, which enables the data to be delivered to the intended node(s). Figure 1.1 shows a PLC system in a VLSI circuit environment. The Test/Control module sends data superimposed on a power line of the system board. The signal travels through a power pin(s), power planes of a package, and the power distribution network and reaches at the intended node(s). The channel characteristics of the power distribution network of a target IC are important to select proper frequency bands, and measured results on channel characteristics of Intel processors are available in [6].

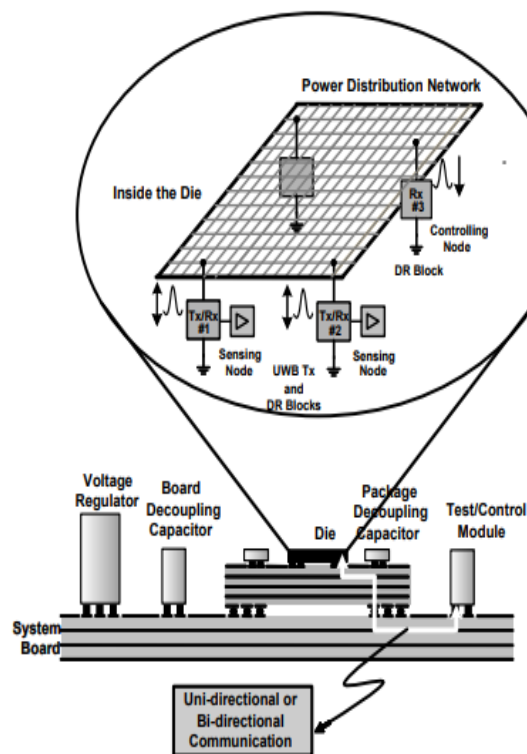


Figure 1.1: Power line communication system in a VLSI circuit

The proposed topic of the thesis research is to develop a PLC receiver in CMOS technology. A few of PLC receivers in CMOS were developed by Dr. Dong S. Ha's team [8]- [10]. The PLC receivers demonstrate feasibility of power line communications in ICs. The PLC receiver proposed by Thirugnanam

et al. in [8] is composed of a sensing circuit, a differential amplifier with an offset cancellation, and a positive feedback latch. The offset cancellation, which removes the DC voltage of the signal, is based on a fixed bias voltage, and is sensitive to supply voltage fluctuations. The PLC receiver was designed in CMOS 0.18 μm technology. The PLC receiver proposed by Chawla et al. in [9] adopts a coherent detection for ultra wideband (UWB) data signals. It achieves a higher sensitivity than its predecessor owing to the coherent detection, but dissipates more power due to higher circuit complexity. Like its predecessor, the PLC receiver also relies on a fixed bias voltage to remove the DC voltage from the signal and hence suffers from the same shortcoming. The PLC receiver was designed in CMOS 0.18 μm technology initially, and was also developed in 0.13 μm CMOS technology later [10]. The supply voltage of an IC varies spatially across the IC as well as in time. Supply voltage may vary because of the non-ideal voltage regulator, IR drop, Ldi/dt noise, and varying power consumption of blocks connected to the same power line. Figure 2.1 shows a supply voltage map indicating the worst case voltage droop on a chip [11]. The map indicates that the supply voltage droop ranges from 3 to 15% of VDD across the chip area. The problem could be worsened for devices powered by batteries as the battery voltage drops over the operating period. Therefore, supply voltage fluctuation is critical issue for IC design.

PLC DESIGN:

The first block is a level shifter, which lowers the DC level of the signal superimposed on the supply voltage, so that the level-shifted signal can be processed by the following signal extractor. The subsequent block, a signal extractor, amplifies the signal and converts it to a differential signal. The logic restorer, which is a Schmitt trigger, recovers logic values from the analog signal. The logic restorer has a differential input and translates the sensed analog signal into a logic value based on the threshold of its hysteresis.

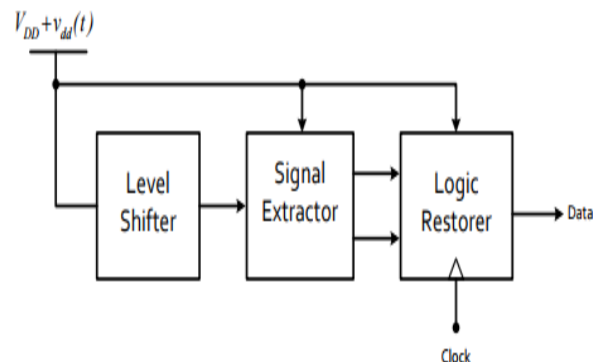


Figure 2.1: Block diagram of the proposed PLC receiver

LEVEL SHIFTER :

The level shifter adopts the common source amplifier with a diode-connected load as shown in Figure 2.2, in which V_{in} is a fixed bias voltage. The level shifter propagates the data signal $v_{dd}(t)$ imposed on the supply voltage V_{DD} to the output, while lowering the DC voltage level of the signal $v_{dd}(t)$ to one half of V_{DD} .

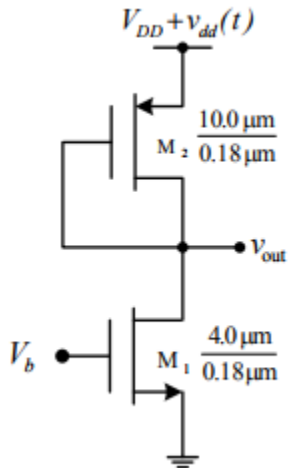


Figure 2.2: Level shifter

To propagate the data signal superimposed on the power line to the output, the output should be sensitive to power supply variations. In other words, contrary to typical amplifier design, the PSRR of the level shifter should be set to small. The PSRR of the level shifter given in (2.5) is shown again below.

$$PSRR = -\frac{g_{m1}}{g_{m2}} = -\frac{\mu_n (W/L)_1 (V_{GS} - V_{th})_1}{\mu_p (W/L)_2 (V_{GS} - V_{th})_2}$$

Equation (2.1) shows that the PSRR can be lowered through a small W/L and a small overdrive voltage of $M1$ and a large W/L and a large overdrive voltage of $M2$. As the desired DC voltage level at the output of the sensing circuit is fixed at $0.5V_{DD}$, which in turn fixes the overdrive voltage of $M2$. Also, the W/L ratio for $M2$ is compromise between the minimum current I_D and a low PSRR. The bias voltage and the W/L ratio of the $M1$ are calculated to ensure that $M1$ remains in saturation. The overdrive voltage ($V_{GS} - V_{TH}$) for the level shifter is set to a near minimal ($= 0.08$ V), $(W/L)M1$ relatively small ($= 22.2$), and $(W/L)M2$ relatively large ($= 55.6$). The level shifter is designed in CMOS $0.18 \mu m$ technology under 1.8 V supply. The parameter values of $M1$ are, $V_{GS} = 0.622$ V, and $V_{th} = 0.537$ V, which result in g_{m1} of 1.002

mS. The parameter values for $M2$ are $|V_{GS}| = 0.723$ V, and $|V_{th}| = 0.556$ V to result in g_{m2} of 0.794 mS. The PSRR for the level shifter is obtained as 1.3 (or 2.27 dB), which is small compared to a typical value ranging from 65.0 dB to 80.0 dB for analog IC.

SIGNAL EXTRACTOR :

The output of the level shifter is the data signal with a DC value of $0.5V_{DD}$. The following signal extractor amplifiers and extracts the signal, while removing the DC voltage of the signal. The signal extractor shown in Figure 2.4 is a differential amplifier, in which one input has a RC low-pass filter. The low-pass filter extracts the DC value of the signal, which can possibly vary or fluctuate, while removing the signal ideally. The differential amplifier removes the DC value, which is common for both inputs. The differential amplifier also converts a single ended input into a differential output

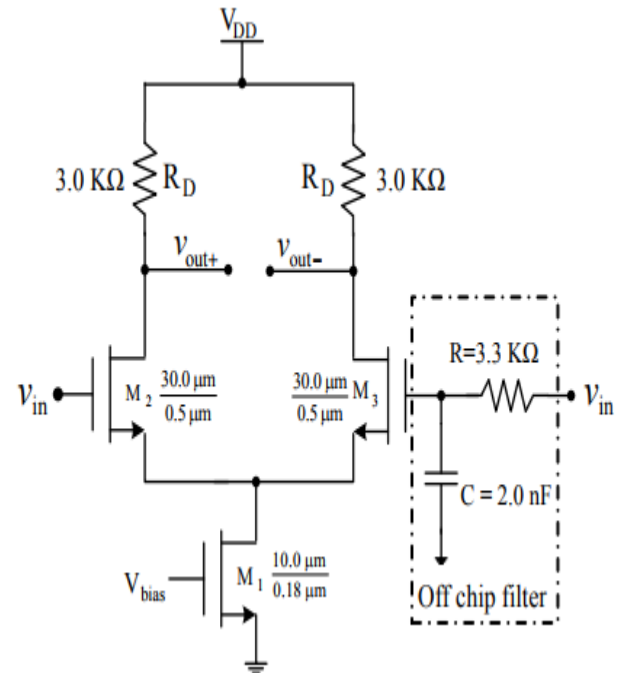


Figure 2.3: Signal extractor

The voltage gain of the differential amplifier is expressed as below. $A_v = g_{m2} / 3R_D$ (2.2) where $g_{m2} = g_{m3}$ and can be expressed as $g_m = \mu_n C_{ox} W/L (V_{GS} - V_{th})$. It can be seen from (2.2) that the gain increases by increasing the transconductance, which in turns increases by increasing W/L or by increasing R_D . However, a large device size leads to increased device parasitic capacitances and a die size, and a higher R_D leads to a higher voltage drop to limit the maximum voltage swings. Thus, a trade-off has to be made

between parasitic capacitances and the maximum voltage swing. In our design the size of the transistor is chosen to be reasonably large to avoid an excessively large RD, which reduces the die size. The gain of the differential amplifier is 10.0 dB, which is large enough to amplify the sensed signal to the required level. Also, a large transistor size and a large resistor are desirable to minimize the DC offset voltage at the input side of the amplifier due to mismatching between devices. The DC offset voltage resulting from mismatching is expressed as

$$V_{OS,in} = \left(\frac{V_{GS} - V_{th}}{2} \right) \sqrt{\left(\frac{\Delta R_D}{R_D} \right)^2 + \left(\frac{\Delta(W/L)}{(W/L)} \right)^2} + \Delta V_{th}^2$$

shows that a large the transistor size and a resistor reduce the DC offset voltage. The RC filter passes the DC and low frequency terms, while removing the signal ideally. So that only the data signal appears at the differential output. The filter is off-chip for our test chip, but can be implemented on chip in the final design. The resistor R of the filter is set to 3.0 KΩ, and the capacitor 5.0 pF for our experiments. The -3 dB cutoff frequency of the RC filter is 10.6 KHz, which is considerably low.

LOGIC RESTORER:

The logic restorer translates the data in analog differential signal form into logic values. It is based on the Schmitt trigger described in Section 2.5. The logic restorer and its transistor sizes are shown in Figure 2.4. A key aspect of the Schmitt trigger is the hysteresis through the regenerative feedback circuit, which is a cross-coupled inverter pair. The transistor size of the inverter pair, specifically M7, and M8, are smaller compared with M1 and M2, so that transistors M1 and M2 have more influence on the current. When a new data signal is applied to the logic restorer, the clock is turned to high to turn off M5 and M6 (which are voltage controlled current sources). The cross-coupled inverter pair settles to a high or low state and the output of the logic restorer is interpreted as a logic value according. Then, the clock signal becomes low, M5 and M6 are turned on. The gap between the high and the low switching voltages of the Schmitt trigger becomes wider due to the additional current supplied by the two transistors. Hence, it requires a larger differential voltage to change the state of the inverter pair, which increases the immunity to noise and disturbances. It should be noted that the sizes of all the transistors were determined through simulations.

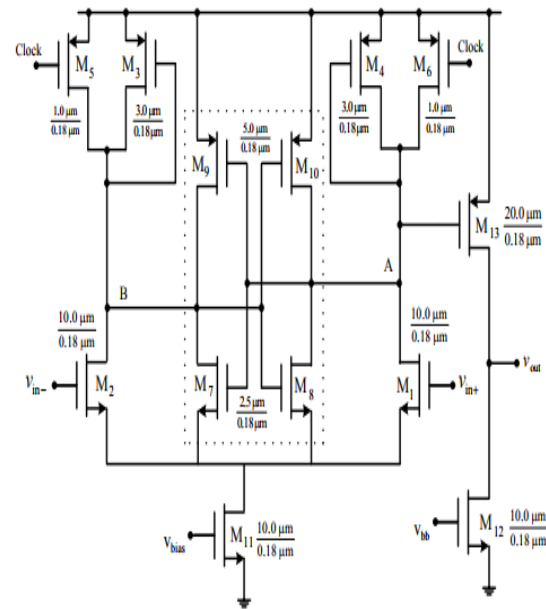
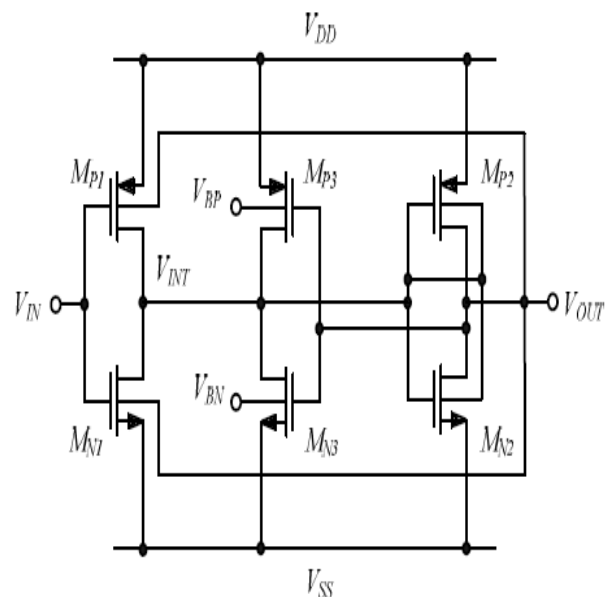


Figure 2.4: A differential Schmitt trigger with the tunable hysteresis

We verified operation of the logic restorer through simulations. We fixed Vin- to a certain reference voltage called Vref for our simulations. Let the cross-coupled inverter pair be deactivated. If Vin+ is equal to Vref, then VA is equal to VB. The voltage transfer characteristic for the circuit under Vref = 1.1V is shown in Figure. Note that the switching voltage is Vin+ is equal to Vref = Vin- = 1.1 V. Suppose that the inverter pair becomes active at the moment.

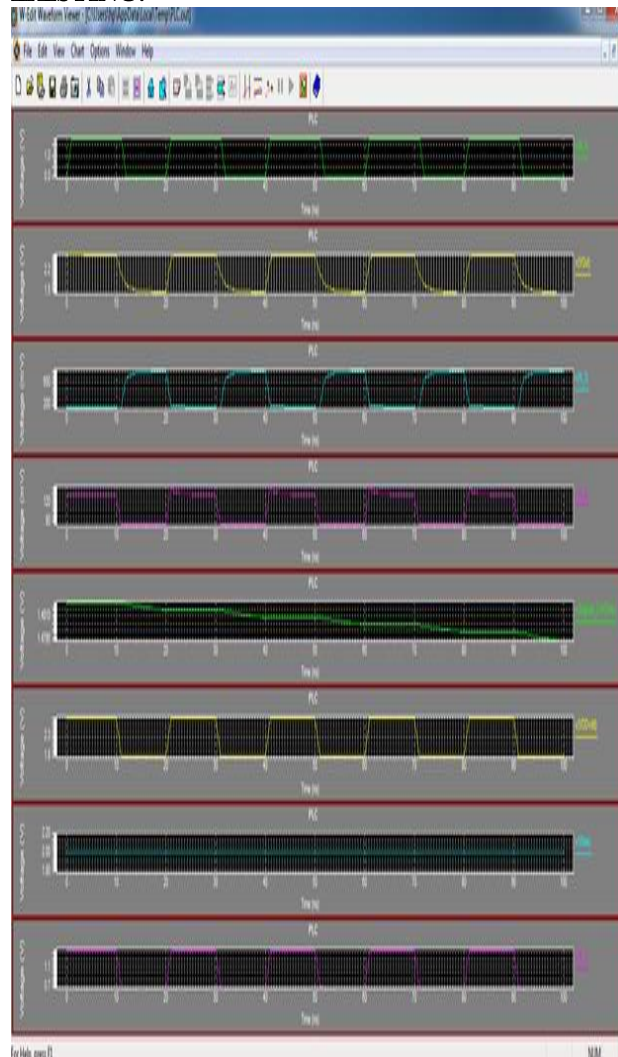
MODIFIED SCHMITT TRIGGER:



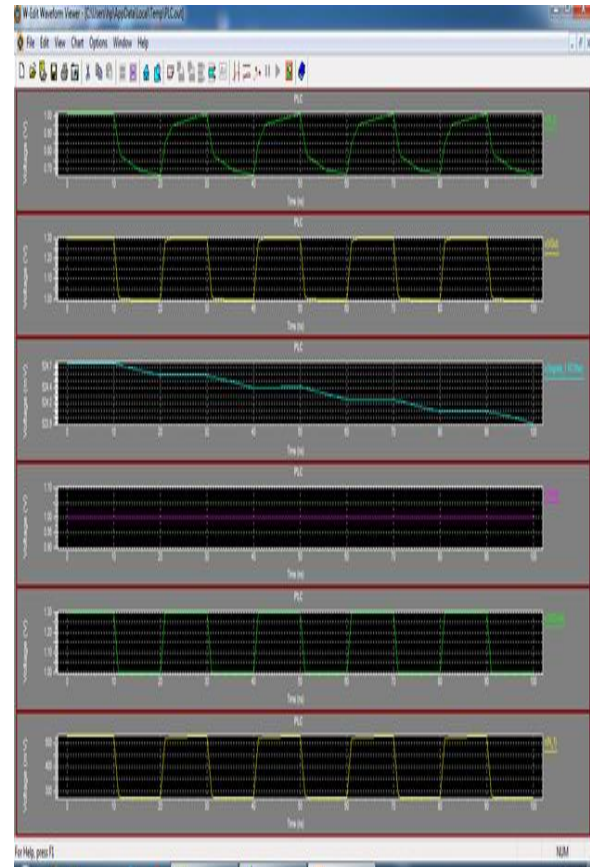
The circuit consists of three stage CMOS inverters. As seen, the first stage CMOS inverter is configured the same as that of existing Schmitt trigger, i.e., dynamic-body bias is used to dynamically adjust the threshold voltage of the transistors $MN1$ and $MP1$, thus the switching threshold of the inverter. The second and third stages are connected as cross-coupled inverters. Transistors $MN2$ and $MP2$ perform a similar function as transistors $MN2$ and $MP2$, while the third stage inverter ($MN3$ and $MP3$) are added to serve two purposes. First, the third and second stage CMOS inverters are connected in a positive feedback configuration, thus speeding up the switching process. Second, the control voltages of the third stage CMOS inverter control the intensity of the feedback signal, thus the switching threshold voltage of the Schmitt trigger.

RESULT:

EXISTING:



PROPOSED:



CONCLUSION:

The proposed PLC receiver was designed and fabricated with low power technology. Measurement results of the three sub-blocks and the entire PLC receiver were presented and reduced compared with the simulation results. In this paper, we presented the feasibility for dual use of power pins, data communications as well as its intended purpose of delivery of power, based on the ultra wideband communication technology and the direct-sequence code division multiple access scheme. Our simulation results indicate that the proposed approach is quite feasible and can be applied to existing packages without or little modification. Further research including design of data recovery blocks and determination of various design parameters is necessary to deploy the proposed method to real world chips.

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